SLG3NT3342

32.768 kHz and MHz GreenCLK

General Description

The SLG3NT3342 is the second generation of the GreenCLK technology that uses a 25 MHz Reference Crystal to provide two 32.768 kHz clock outputs, two 25 MHz clock outputs, and one 12 MHz clock output. The part supports a non-rechargeable or rechargeable coin cell battery (ex. CR2032 or ML 1220) as the power source for the ultra low power Hibernate mode operation.

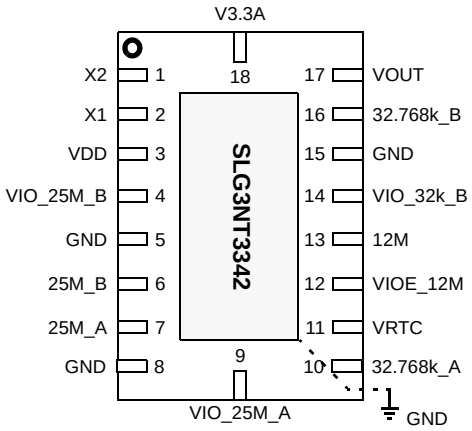
Features

- 32.768k_A: 32.768 kHz GreenCLK 2 technology for RTC
- 25M_A: 3.3 V swing 25 MHz for LAN REFCLK
- 25M_B: 1.05 V swing 25 MHz for Intel PCH
- 12M: 12 MHz without spread
- Scalable VIO for 32.768k_B, 25M_B, and 12M
- Improved performance over temperature
- Supports Industrial temperature range
- No 32.768 kHz tuning fork crystal
- Removes up to 11 components from a standard notebook and/or netbook design
- Smaller package and layout foot print
- 18-pin TQFN: 2 x 3.5 x 0.75 mm, 0.4 mm pitch
- Pb-Free / Halogen-Free / RoHS compliant

Output Summary

- 2x 32.768 kHz clock outputs (1.5 µA in Hibernate Mode)
- 2x 25 MHz clock outputs (1.5 mA in Active Mode)
- 1x 12 MHz clock output (11 mA in Active Mode)

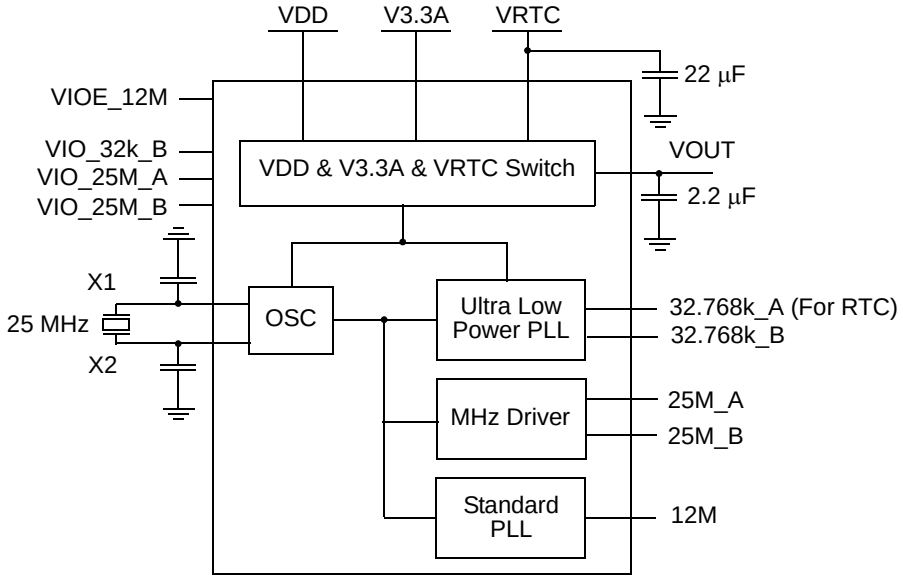
Pin Configuration



18-pin TQFN

(Top View)

Block Diagram



Pin Description

Pin #	Pin Name	Type[1]	Pin Description[2]
1	X2	O, SE	**Crystal Interface:** 25 MHz, OSC output
2	X1	I	**Crystal Interface:** 25 MHz, OSC input
3	VDD	PWR	**Power Supply:** 3.3 V for Active Mode
4	VIO_25M_B	PWR	**Power Supply:** Power for 25M_B output
5	GND	GND	**Ground**
6	25M_B	O, SE	**Clock Output:** 25 MHz output (Stop by $V_{IO\_25M\_B}$)
7	25M_A	O, SE	**Clock Output:** 25 MHz output (Stop by $V_{IO\_25M\_A}$)
8	GND	GND	**Ground**
9	VIO_25M_A	PWR	**Power Supply:** Power for 25M_A output
10	32.768k_A	O, SE	**Clock Output:** 32.768 kHz output for RTC (Free Running)
11	VRTC	PWR	**Power Supply:** Power for 32.768 kHz output. Connect to a non-rechargeable or rechargeable coin cell battery[3,4] (ex. CR2032 or ML1220). 32.768 kHz (32.768k_A) clock will draw power from this pin during Hibernate Mode (when $V_{3.3A}$ = 0 V and V_{DD} = 0 V). 22 µF decoupling capacitor is recommended.
12	VIOE_12M	PWR	**Power Supply:** Serves as power for 12M output as well as enable signal for the Standard PLL
13	12M	O, SE	**Clock Output:** 12 MHz output from Standard PLL (Stop by V_{IOE_12M})
14	VIO_32k_B	PWR	**Power Supply:** Power for 32.768k_B output
15	GND	GND	**Ground**
16	32.768k_B	O, SE	**Clock Output:** 32.768 kHz output (Stop by $V_{IO\_32k\_B}$)
17	VOUT	PWR	**Power Output:** 2.2 µF decoupling capacitor is recommended.
18	V3.3A	PWR	**Power Supply:** Power for 32.768 kHz outputs. Both 32.768 kHz (32.768k_A and 32.768k_B) clocks will draw power from this pin during Active and/or Suspend Mode (when $V_{3.3A}$ = 3.3 V).
Exposed Bottom Pad	GND	GND	**Ground**

Notes:

1. Type Definitions
   - PWR: power
   - GND: ground
   - I: input
   - O: output
   - SE: single ended signal
2. It is recommended that all Power Supply pins have a decoupling capacitor attached (0.1 µF minimum).
3. When CR coin cell battery is used, place a 301 Ω resistor between the coin cell and the decoupling capacitor to meet the UL safety requirement.
4. When ML coin cell battery is used, place a 100 Ω resistor between the coin cell and the decoupling capacitor to meet the UL safety requirement.

Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
V_{DD}	Voltage on VDD pin relative to GND	-0.3	4.2	V
$V_{3.3A}$	Voltage on V3.3A pin relative to GND	-0.3	4.2	V
V_{RTC}	Voltage on VRTC pin relative to GND	-0.3	4.2	V
T_S	Storage Temperature	-65	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	--	2000	V
MSL	Moisture Sensitivity Level	1		

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature

Parameter	Description	Min.	Max.	Unit
T_O	Operating Temperature	-40	85	°C

Recommended 25 MHz Reference Crystal Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	25	--	MHz
F_{ERRI}	Frequency Accuracy	@ 25 °C	--	--	±10	ppm
F_{ERRT}	Frequency Error over Temperature	@ -40 °C to 85 °C	--	--	±10	ppm
F_{AGE}	Frequency Aging	per year	--	--	±1[1]	ppm
DL	Drive Level		--	--	100	µW
C_L	Crystal Load Capacitance	Parallel Resonance	8			pF
AT	AT Cut Crystal		--	--	--	
Mode	Fundamental		--	--	--	

Notes:
1. Vendor Specific: Frequency aging may be different per crystal used. Check with crystal vendor for specific value. SLG3NT3342 outputs will track the crystal frequency aging as stated in other sections of this datasheet.

32.768 kHz Clock Output Characteristics (32.768k_A & 32.768k_B in Hibernate/Suspend Mode)

T_A = 25 °C, V_{RTC} = 2.9 V, ($V_{3.3A}$ = 3.3 V for Suspend Mode) (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$32F_{INI}$	Initial Frequency		--	32.768	--	kHz
$32F_{ERRI}$[1]	Frequency Error at Room Temperature	@ 25 °C	--	±17	±23.0	ppm
			--	±1.5	±2.0	sec/day
$32F_{ERRT}$[1]	Frequency Error over Operating Temperature Range	@ -40 °C to 85 °C	--	±24.2	±34.5	ppm
			--	±2.1	±3.0	sec/day
$32F_{AGE}$	Frequency Aging	per year	Reference Crystal[2]			ppm
DC	Duty Cycle	0.5 V for 32.768k_A; 0.5 x $V_{IO\_32k\_B}$ for 32.768k_B	45	50	55	%
V_{OH}	Output Voltage HIGH	for 32.768k_A	0.8	1.0	1.2	V
		for 32.768k_B	0.8 x $V_{IO\_32k\_B}$	--	--	V
V_{OL}	Output Voltage LOW	for 32.768k_A	--	--	0.3	V
		for 32.768k_B	--	--	0.2 x $V_{IO\_32k\_B}$	V

Notes:
1. a. Respective values for this parameter is guaranteed only when the recommended 25 MHz Reference Crystal is used, and the values take into account the crystal variations.
   b. Assumes crystal ppm spec is a σ or Gaussian distribution.
   c. Assumes crystal load capacitors are within ±5% of ideal value.
   d. Assumes measurement is 7 day average.
2. This parameter tracks Reference Crystal characteristics.

32.768 kHz Clock Output Characteristics (32.768k_A & 32.768k_B in Active Mode)

T_A = 25 °C, V_{RTC} = 2.9 V, $V_{3.3A}$ = 3.3 V, V_{DD} = 3.3 V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$32F_{INI}$	Initial Frequency		--	32.768	--	kHz
$32F_{ERRI}$	Frequency Error at Room Temperature	@ 25 °C	Reference Crystal[1]			ppm
$32F_{ERRT}$	Frequency Error over Operating Temperature Range	@ -40 °C to 85 °C	Reference Crystal[1]			ppm
$32F_{AGE}$	Frequency Aging	per year	Reference Crystal[1]			ppm
DC	Duty Cycle	0.5 V for 32.768k_A; 0.5 x $V_{IO\_32k\_B}$ for 32.768k_B	45	50	55	%
V_{OH}	Output Voltage HIGH	for 32.768k_A	0.8	1.0	1.2	V
		for 32.768k_B	0.8 x $V_{IO\_32k\_B}$	--	--	V
V_{OL}	Output Voltage LOW	for 32.768k_A	--	--	0.3	V
		for 32.768k_B	--	--	0.2 x $V_{IO\_32k\_B}$	V

Notes:
1. This parameter tracks Reference Crystal characteristics.

25 MHz Clock Output Characteristics (25M_A)

T_A = 25 °C, V_{RTC} = 2.9 V, $V_{3.3A}$ = 3.3 V, V_{DD} = 3.3 V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	25	--	MHz
F_{ERRI}	Frequency Error at Room Temperature	@ 25 °C	Reference Crystal[1]			ppm
F_{ERRT}	Frequency Error over Operating Temperature Range	@ -40 °C to 85 °C	Reference Crystal[1]			ppm
F_{AGE}	Frequency Aging	per year	Reference Crystal[1]			ppm
DC	Duty Cycle	0.5 x $V_{IO\_25M\_A}$	45	50	55	%
V_{OH}	Output Voltage HIGH	I_{OH} = 1 mA	0.8 x $V_{IO\_25M\_A}$	--	--	V
V_{OL}	Output Voltage LOW	I_{OL} = -1 mA	--	--	0.2 x $V_{IO\_25M\_A}$	V

Notes:
1. This parameter tracks Reference Crystal characteristics.

25 MHz Clock Output Characteristics (25M_B)

T_A = 25 °C, V_{RTC} = 2.9 V, $V_{3.3A}$ = 3.3 V, V_{DD} = 3.3 V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	25	--	MHz
F_{ERRI}	Frequency Error at Room Temperature	@ 25 °C	Reference Crystal[1]			ppm
F_{ERRT}	Frequency Error over Operating Temperature Range	@ -40 °C to 85 °C	Reference Crystal[1]			ppm
F_{AGE}	Frequency Aging	per year	Reference Crystal[1]			ppm
DC	Duty Cycle	0.5 x $V_{IO\_25M\_B}$	45	50	55	%
V_{OH}	Output Voltage HIGH	I_{OH} = 1 mA	0.8 x $V_{IO\_25M\_B}$	--	--	V
V_{OL}	Output Voltage LOW	I_{OL} = -1 mA	--	--	0.2 x $V_{IO\_25M\_B}$	V

Notes:
1. This parameter tracks Reference Crystal characteristics.

12 MHz Clock Output Characteristics (12M)

T_A = 25 °C, V_{RTC} = 2.9 V, $V_{3.3A}$ = 3.3 V, V_{DD} = 3.3 V (unless otherwise stated)

Symbol	Description	Conditions	Min	Typ	Max	Unit
F_{INI}	Initial Frequency		--	12	--	MHz
F_{ERRI}	Frequency Error at Room Temperature	@ 25 °C	Reference Crystal[1]			ppm
F_{ERRT}	Frequency Error over Operating Temperature Range	@ -40 °C to 85 °C	Reference Crystal[1]			ppm
F_{AGE}	Frequency Aging	per year	Reference Crystal[1]			ppm
DC	Duty Cycle	0.5 x V_{IOE_12M}	45	50	55	%
V_{OH}	Output Voltage HIGH	I_{OH} = 1 mA	0.8 x V_{IOE_12M}	--	--	V
V_{OL}	Output Voltage LOW	I_{OL} = -1 mA	--	--	0.2 x V_{IOE_12M}	V
t_{LCK}	Standard PLL Lock Time	VIOE_12M to 12M	1	--	3	ms

Notes:
1. This parameter tracks Reference Crystal characteristics.

Power Supply Electrical Specifications (VDD, V3.3A, VRTC, and VIO)

T_A = 25 °C

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage for VDD	Active Mode	3.0	3.3	3.6	V
$V_{3.3A}$	Operating Voltage for V3.3A	Active/Suspend Mode	3.0	3.3	3.6	V
V_{RTC}	Operating Voltage for VRTC	In any Mode	2.3	2.9	3.0	V
$V_{IO\_32k\_B}$	Operating Voltage for VIO_32k_B	Active/Suspend Mode	0.9975	3.3	3.6	V
$V_{IO\_25M\_A}$	Operating Voltage for VIO_25M_A	Active Mode	3.0	3.3 [2]	3.6	V
$V_{IO\_25M\_B}$	Operating Voltage for VIO_25M_B	Active Mode	0.9975	1.05 [3]	1.575	V
V_{IOE_12M}	Operating Voltage for VIOE_12M	Active Mode	1.6	3.3	3.6	V
V_{SW} [4]	V_{DD} trip point for Active Mode Entry and Exit		1.7	--	2.1	V
I_{VRTC} [1]	V_{RTC} current consumption in Hibernate Mode	V_{DD} = 0 V, $V_{3.3A}$ = 0 V, V_{RTC} = 2.9 V	--	1.5	--	µA
$I_{V3.3A}$ [1]	$V_{3.3A}$ current consumption in Active and/or Suspend Mode	V_{DD} = 3.3 V or 0 V, $V_{3.3A}$ = 3.3 V, V_{RTC} = 2.9 V	--	7	--	µA
I_{VDDA} [1,5]	V_{DD} current consumption in Active Mode with Standard PLL in Power Down Mode	V_{DD} = 3.3 V, $V_{3.3A}$ = 3.3 V, V_{RTC} = 2.9 V, V_{IOE_12M} = 0 V	--	1.5	--	mA
I_{VDDAP} [1,6]	V_{DD} current consumption in Active Mode with Standard PLL Enabled	V_{DD} = 3.3 V, $V_{3.3A}$ = 3.3 V, V_{RTC} = 2.9 V, V_{IOE_12M} = 3.3 V	--	11	--	mA
V_{OUT}	VOUT Output Voltage Level	Hibernate Mode	V_{RTC} - 0.5	V_{RTC} - 0.4	V_{RTC} - 0.3	V
		Active/Suspend Mode	$V_{3.3A}$ - 0.5	$V_{3.3A}$ - 0.4	$V_{3.3A}$ - 0.3	V
I_{OUT} [1]	Current Output on VOUT	In any Mode	--	2.5	6	µA

Notes:
1. Average current depends on application and output load. Specified values are for No Load condition.
2. Recommended as the clock source for a LAN controller.
3. Recommended as the clock source for the Intel PCH or ICH.
4. V_{SW} range includes hysteresis of ±50 mV.
5. All outputs are active except the output from the Standard PLL.
6. All outputs are active including the output from the Standard PLL.

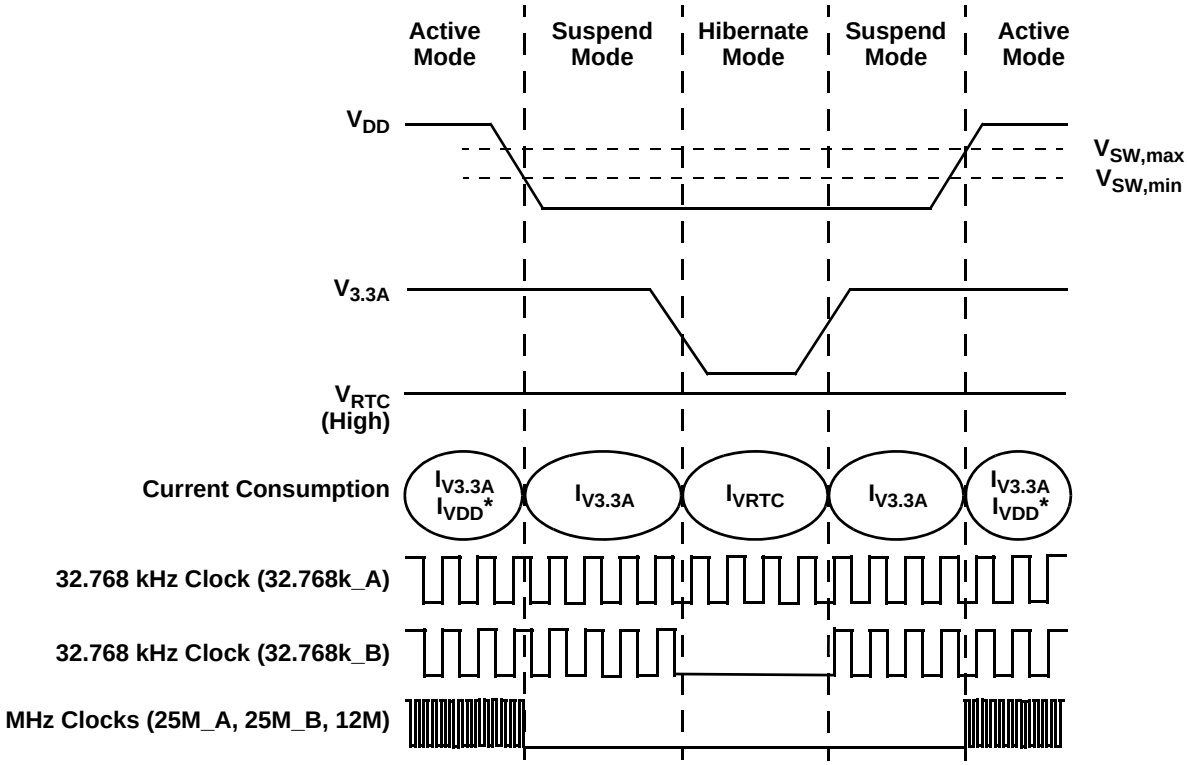
Full State Table: Power Modes, Power Supply & Output Controls per Clock Output Functions

Power Mode (Power State)	Power Supply[1] & Output Control[2,5]							Clock Output & V_{OUT} (typ)						Current (typ)		
	V_{RTC}	$V_{3.3A}$	V_{DD}	$V_{IO\_32k\_B}$	$V_{IO\_25M\_A}$	$V_{IO\_25M\_B}$	V_{IOE_12M}	32.768k_A	32.768k_B	25M_A	25M_B	12M	V_{OUT} [V]	I_{VRTC} [µA]	$I_{V3.3A}$ [µA]	I_{VDD} [mA][6]
Hibernate Mode	H	L[4]	L[4]	L[4]	L[4]	L[4]	L[4]	ON	OFF	OFF	OFF	OFF	V_{RTC} - 0.4	1.5	0	0
Suspend Mode	H	H	L[4]	L	L[4]	L[4]	L[4]	ON	OFF	OFF	OFF	OFF	$V_{3.3A}$ - 0.4	0	7	0
				H					ON							
Active Mode w/ PLL PD	H	H	H	L	V	V	L	ON	OFF	--[3]	--[3]	OFF	$V_{3.3A}$ - 0.4	0	7	1.5
				H					ON							
				V	L	V			--[3]	OFF	--[3]					
					H					ON						
				V	V	L			--[3]	--[3]	OFF					
						H					ON					
Active Mode w/ PLL Enabled	H	H	H	L	V	V	H	ON	OFF	--[3]	--[3]	ON	$V_{3.3A}$ - 0.4	0	7	11
				H					ON							
				V	L	V			--[3]	OFF	--[3]					
					H					ON						
				V	V	L			--[3]	--[3]	OFF					
						H					ON					

Notes:

1. Refer to the Power Supply Electrical Specifications (VDD, V3.3A, VRTC, and VIO) for respective voltage ranges. Please note that (V_{RTC} = H & $V_{3.3A}$ = L & V_{DD} = H) is an illegal condition.
2. States
   - L: Grounded
   - H: Powered
   - V: Valid, must be L or H
3. This output could be ON or OFF depending on the associated V_{IO}.
   - ON: when V_{IO} = H
   - OFF: when V_{IO} = L
4. May be floated.
5. VDD power up (L to H) should always precede VIOE_12M transition (L to H) for proper functionality of the Standard PLL.
6. I_{VDD} is either I_{VDDA} or I_{VDDAP} depending on the state(s) of VIOE(s).

Power Mode Switching Diagram

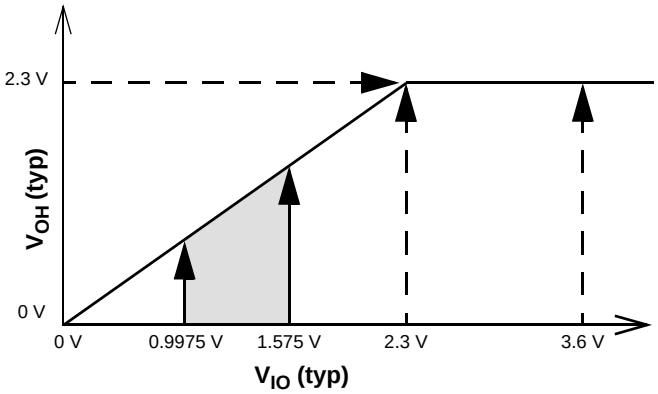


* I_{VDD} is either I_{VDDA} or I_{VDDAP} depending on the state(s) of VIOE(s).

Output Buffer Characteristics

Power Supply Operating Ranges

25M_B: V_{OH}/V_{OL} vs. V_{IO}

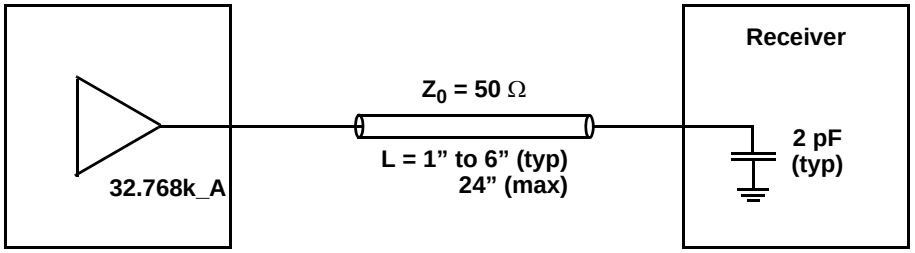


Note: V_{IO} represents $V_{IO\_25M\_B}$

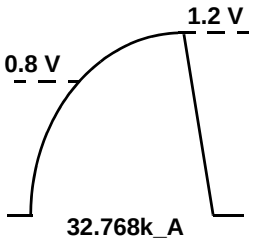
Routing and Loading Recommendations, and Typical Output Waveforms

32.768 kHz Clock Output Buffer (32.768k_A)

Routing and Loading Recommendation

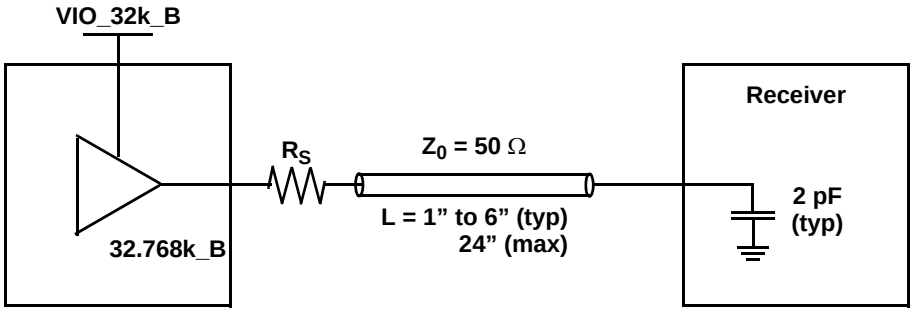


Typical Output Waveform

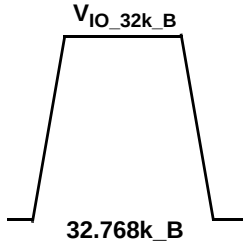


32.768 kHz Clock Output Buffer (32.768k_B)

Routing and Loading Recommendation



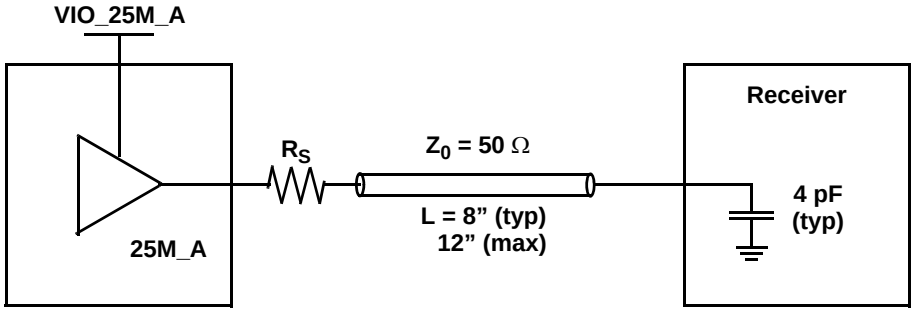
Typical Output Waveform



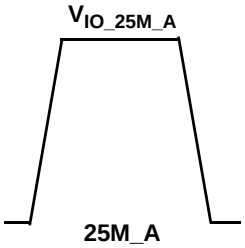
Note: R_S should be tuned to the actual PCB design and choice of $V_{IO\_32k\_B}$ level per application.
General recommendation is R_S = 0 Ω at $V_{IO\_32k\_B}$ = 3.3 V.

25 MHz Clock Output Buffer (25M_A)

Routing and Loading Recommendation



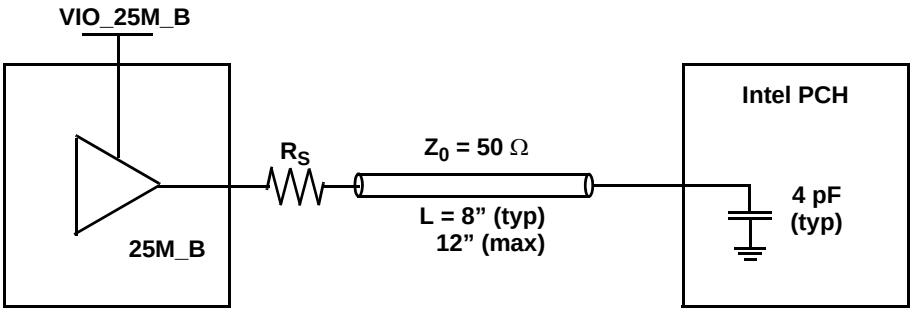
Typical Output Waveform



Note: R_S should be tuned to the actual PCB design and choice of $V_{IO\_25M\_A}$ level per application.
General recommendation is R_S = 33 Ω at $V_{IO\_25M\_A}$ = 3.3 V.

25 MHz Clock Output Buffer (25M_B)

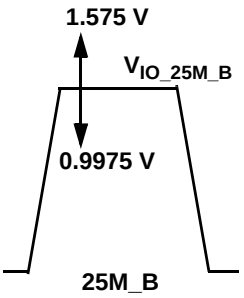
Routing and Loading Recommendation



$V_{IO\_25M\_B}$ of 1.05 V is recommended

Intel PCH only accepts V_{OH} of 0.9975 V to 1.575 V

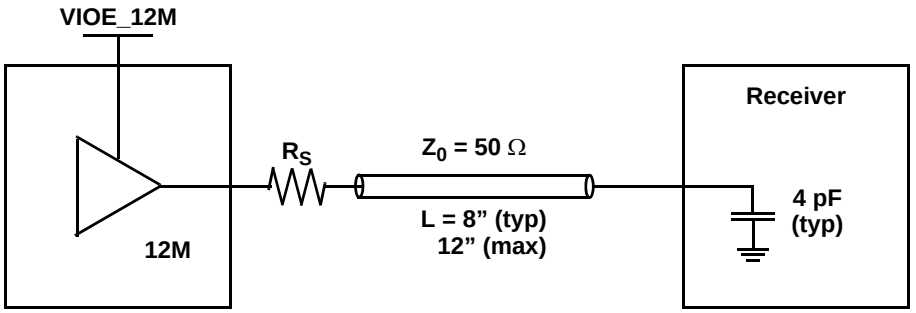
Typical Output Waveform



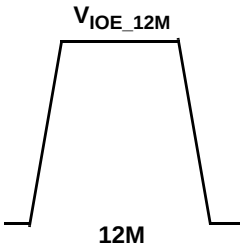
Note: R_S should be tuned to the actual PCB design and choice of $V_{IO\_25M\_B}$ level per application.
General recommendations are R_S = 0 Ω at $V_{IO\_25M\_B}$ = 1.05 V.

12 MHz Clock Output Buffer (12M)

Routing and Loading Recommendation



Typical Output Waveform



Note: R_S should be tuned to the actual PCB design and choice of V_{IOE_12M} level per application.
General recommendations are R_S = 10 Ω at V_{IOE_12M} = 1.8 V, and R_S = 22 Ω at V_{IOE_12M} = 3.3 V.

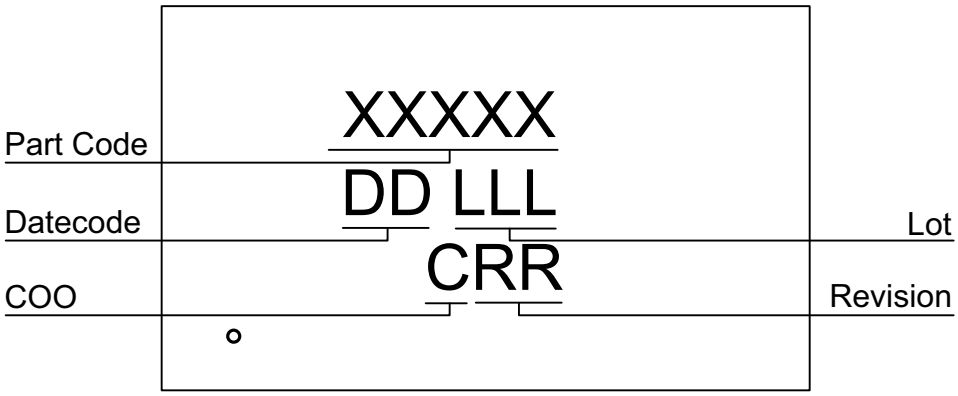
VRTC Battery Recommendations

Non-rechargeable Coin Cell Battery

Battery Part Number	SLG3NT3342 32.768 kHz Lifetime[1] [years]	Capacity[2] [mAH]	Voltage Range[2] [V]			Max Discharge Current[2] [mA]		Dimensions[2] [mm]	
			95%	50%	5%	Constant	Peak	Dia.	Height
CR2032[3]	6.3 to 6.8	220 to 240	3	2.9	2.3	4 to 6	20	20.0	3.2

Notes:
1. Lifetime calculation assumes 4.0 µA (typ) current consumption for 32.768 kHz (RTC) operation, where 4.0 µA (typ) is the sum of 1.5 µA (typ), consumed by the SLG3NT3342 to provide RTC clock, and 2.5 µA (typ), consumed by the RTC logic device (provided via VOUT pin).
2. Exact values depend on the battery manufacturer (Refer to the battery datasheet for details)
3. Lithium Manganese Dioxide non-rechargeable battery

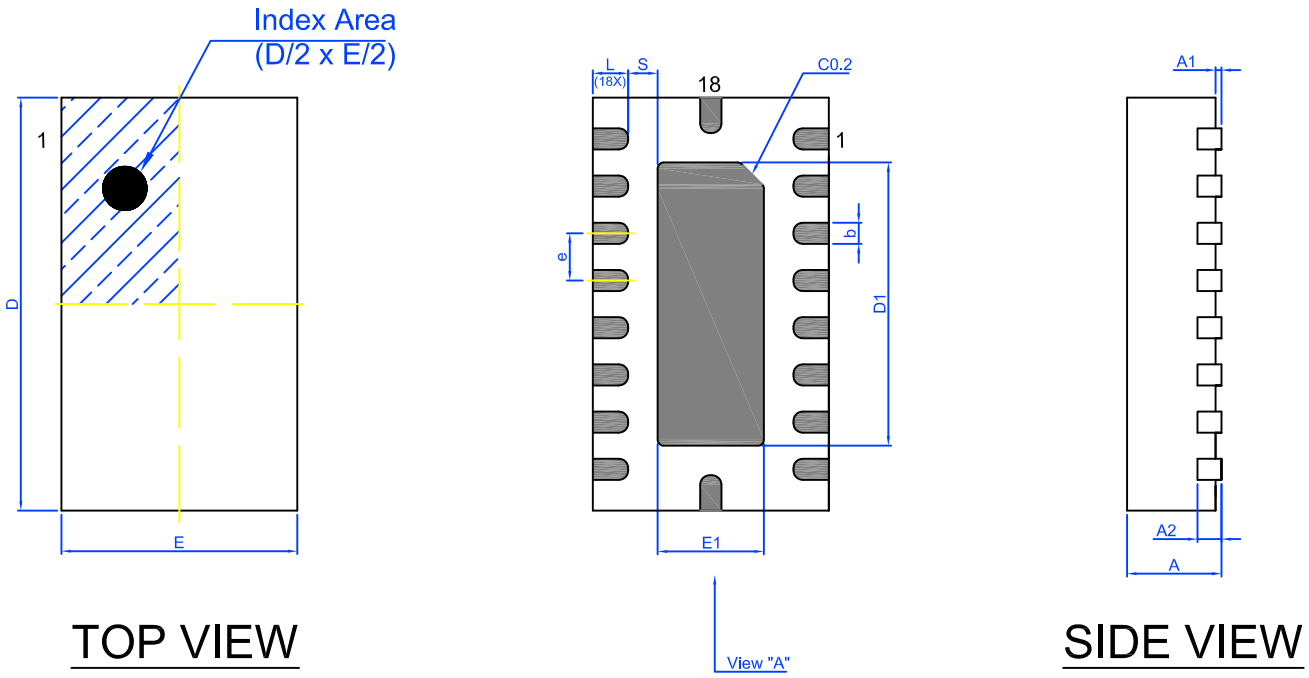
Package Top Marking System Definition



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Package Drawing and Dimensions

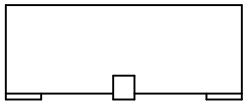
18 Lead TQFN Package
JEDEC MO-220, Variation WCFE



TOP VIEW

BOTTOM VIEW

SIDE VIEW



VIEW "A"

Unit: mm

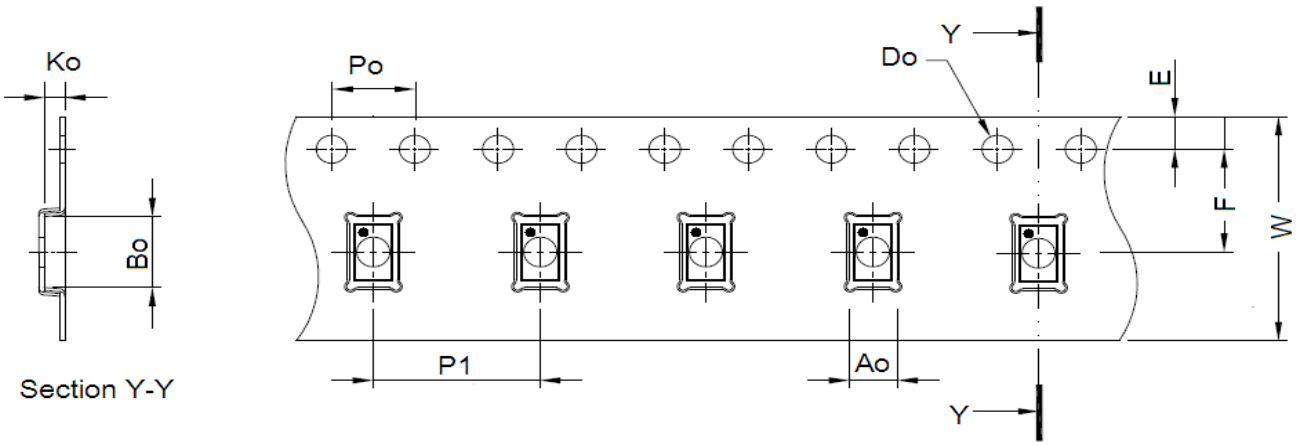
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.700	0.750	0.800	D	3.450	3.500	3.550
A1	0.000	-	0.050	E	1.950	2.000	2.050
A2	0.203 REF			D1	2.35	2.40	2.45
b	0.13	0.18	0.23	E1	0.85	0.90	0.95
e	0.400 BSC			L	0.25	0.30	0.35
S	0.18	-	-				

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TQFN 18L Green	18	2 x 3.5 x 0.75	5,000	10,000	330 / 100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TQFN 18L Green	2.3	3.8	1	4	8	1.5	1.75	5.5	12



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 5.25 mm^3 (nominal). More information can be found at www.jedec.org.

Ordering Information

Part Number	Type	Production Flow
SLG3NT3342V	18-pin TQFN	Industrial, -40 °C to 85 °C
SLG3NT3342VTR	18-pin TQFN (Tape and Reel)	Industrial, -40 °C to 85 °C

Revision History

Date	Version	Change	Page
11/29/2012	1.0	Production release	

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:

http://greenpak.silego.com/
http://greenfet.silego.com/
http://greenpak2.silego.com/
http://greenfet2.silego.com/
http://greenclk.silego.com/

Products are also available for purchase directly from Silego at the Silego Online Store at http://store.silego.com/.

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send e-mail requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

Online Live Support

Silego Technology has live video technical assistance and sales support available at http://www.silego.com/. Please ask our live web receptionist to schedule a 1 on 1 training session with one of our application engineers.

Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL:

http://support.silego.com/

Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of world wide Silego Technology offices and representatives are all available at http://www.silego.com/